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## <u>IN-THE-UNITED-STATES-PATENT-AND-TRADEMARK OFFICE</u>

: Eiki Hashimoto

Serial No

10/015,209

Filed

November 16, 2001

Title

Semiconductor Circuit Designing Apparatus and...

Group Art Unit

2812

\_\_ \_ \_April-30,-2002 \_\_ \_

Attn: Customer Corrections Division Assistant Commissioner for Patents Washington, D.C. 20231

### REQUEST FOR CORRECTED FILING RECEIPT

SIR:

We received the filing receipt on the above-referenced case, copy enclosed,

wherein the FILING DATE was incorrectly listed as: 11/23/2001. Please change the same to read:

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Respectfully submitte

Michael I. Markowitz

Reg. No. 30,659

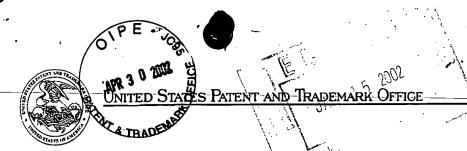
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Docket No.: 100806-00056 (NEKU 19.181)

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COMMISSIONER FOR PATENTS UNITED STATES PATENT AND TRADEMARK OFFICE WASHINGTON, D.C. 20231

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APPLICATION NUMBER

**FILING DATE** 

GRP ART UNIT 2812

FIL FEE REC'D 740

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14

20

TOT CLAIMS

3

10/015,209

11/14/2001

19.181

**DRAWINGS** 

**CONFIRMATION NO. 5984** 

026304 **ROSENMAN & COLIN LLP 575 MADISON AVENUE** <u>NEW YORK, NY 10022-2585</u> **FILING RECEIPT** \*OC000000007285532\*

Date Mailed: 01/10/2002

HAY 13 2002 C 2800 MAIL ROOM

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Eiki Hashimoto, Kanagawa, JAPAN;

Domestic Priority data as claimed by applicant

F reign Applications

JAPAN 354306/2000 11/21/2000

If Required, Foreign Filing License Granted 01/09/2002

**Projected Publication Date: 05/23/2002** 

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor circuit designing apparatus and a semiconductor circuit designing method in which the number of steps in a circuit design and a layout design is reduced

**Preliminary Class** 

438

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